IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) A front-end processing system for a processor, comprising:

a UOP cache and an instruction cache, each having inputs coupled to a common addressing input, the UOP cache having an output for a hit/miss indicator,

an instruction processing system in communication with the instruction cache, having ~~an enabling~~ power control input coupled to the hit/miss output of the UOP cache.

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2. (Currently Amended) The front-end processing system of claim 1, wherein the instruction cache comprises a cache lookup unit and a cache fetch unit, the cache fetch unit having ~~an enabling~~a power control input coupled to the hit/miss output of the UOP cache.

3. (Currently Amended) The front-end processing system of claim 1, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to ~~each other~~the power control input.

4. (Currently Amended) The front-end processing system of claim 1, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit ~~coupled to~~to generate the hit/miss output.

5. (Original) The front-end processing system of claim 4, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit.

6. (Original) The front-end processing system of claim 5, wherein the delay element is associated with a delay corresponding to a processing time of the instruction processing system.

7. (Currently Amended) A cache comprising:

a cache lookup unit,

a delay element having an input coupled to an output of the cache lookup unit, and

a data fetch unit having a power control input coupled to an output of the delay element.

8. (Original) The cache of claim 7, wherein the cache is populated by a plurality of cache entries and wherein the cache lookup unit comprises tag fields of the cache entries and a comparator coupled to the tag fields.

9. (Currently Amended) The cache of claim 8, wherein the cache is populated by a plurality of cache ~~entries~~ ways and wherein the cache lookup unit comprises a tag array for each ~~fields of the~~ cache ways ~~entries~~ and a comparator coupled to each of the tag array. ~~fields.~~

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10. (Currently Amended) A front-end processing system for a processor, comprising:

a UOP cache and an instruction cache, each having inputs coupled to a common addressing input, wherein the UOP cache includes an output for a hit/miss indicator,

wherein the instruction cache includes a cache lookup unit and a data fetch unit, the hit/miss indicator to ~~selectively disable~~ unpower the data fetch unit selectively.

11. (Currently Amended) The front-end system of claim 10, further comprising an instruction processing system in communication with the instruction cache, the hit/miss indicator to ~~selectively disable~~unpower the instruction processing system selectively.

12. (Currently Amended) The front-end processing system of claim 11, wherein the instruction processing system comprises an instruction synchronizer and an instruction decoder coupled to ~~each other~~the hit/miss indicator.

13. (Original) The front-end processing system of claim 10, wherein the UOP cache comprises a cache lookup unit and a cache fetch unit, the cache lookup unit coupled to the hit/miss indicator.

14. (Currently Amended) The front-end processing system of claim 13, wherein the UOP cache further comprises a delay element provided between the cache lookup unit and the cache fetch unit, the delay element to be controlled by the hit/miss indicator.

15. (Currently Amended) The front-end processing system of claim 14, wherein the delay element is ~~associated with~~characterized by a delay corresponding to a processing time of the instruction processing system.

16.-22. Canceled.

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Please add the following new claims:

23. (New) The cache of claim 7, wherein the delay element is to delay operation of the data fetch unit to be synchronized to a timing scheme of an external data input device.

24. (New) The cache of claim 7, wherein the delay element is a multi-cycle delay element.

25. (New) The cache of claim 7, wherein:

the cache lookup unit is to generate a hit/miss indicator in response to an input address, and

the delay element is to become opaque in response to a miss indicator.

26. (New) A cache system, comprising:

a first cache sub-system comprising the cache of claim 7, and

a second cache system characterized by a longer response time than the cache lookup unit and data fetch unit of the first cache sub-system,

wherein the delay element is characterized by a delay equal to a difference between the response time of the second cache sub-system and the response times of the cache lookup unit and data fetch unit.